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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,513	08/17/2001	Yves Morand	00-CCL-096	6322

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EXAMINER	
LEE, HSIEN MING	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 09/25/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/932,513	MORAND ET AL.
	Examiner	Art Unit
	Hsien-Ming Lee	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 17 August 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2, 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1, 3, 4, 6, 7, 8, 10, 11 are generally narrative, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document. The limitations are considered " negatively recited processing steps", which fails to conform with current U.S. practice.

3. Claims 1, 3, 4, 6-8, 10-13, 15, 17 and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The way of describing the invention as in claims 1, 4, 7, 8 and 11 are confusing to the Examiner. For example, what does it mean " the simultaneously production, in at least part of an intertrack insulating layer associated with a given metallization level, on the other hand, of the two electrodes and of the dielectric layer of the capacitor and, on the other hand, of a conducting trench which laterally extends the lower electrode of the capacitor" (claim 1) and where is the exact location of " auxiliary trench" (claim 7) with respect to the "conducting trench" (claim 1) ? What does it mean " less than twice the sum of the thickness of the first conducting layer and of the thickness of the dielectric layer " ? (claim 8, lines 14-15) Rephrasing the entire claims 1, 4, 7, 8 and 11 based on current U.S. practice is needed.

The descriptions of claims 3, 6 10, 12, 13, 15, 17 and 18 are not well understood to the Examiner. Does it mean that simultaneously forming the metallization (90) and the upper

electrode (70) as shown in Figs. 10-11 ? (refers to claims 3, 6, 10) And which metallization level is referred to " the given metallization" ? (refers to claims 3, 6, 13, 15, 17; claim 12, line 6; claim 18, line 8)

4. Claim 2 recites the limitation "the first electrode " in line 2; and " the internal walls" in line 19. Claim 4 recites the limitation "the etching" in line 5; and " the internal walls" in line 19. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

6. Claims 1, 2, 4, 5, 7 and 12-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Brabazon et al. (US 6,008,083).

With respect to claims 1, 2, Brabazon et al identically teach the claimed method for fabricating an integrated circuit, the method comprising the steps of :

- forming a plurality of metallization levels, i.e. first metallization level 10, second metallization level 54, 56 and third metallization level 74, 76, 78, wherein each of the metallization levels are separated by interlevel insulating layer 52 (Fig.13);

- forming the intertrack insulating layer 72 to insulate each track of the same metallization level, i.e. forming the layer 72 to insulate the metallization 74, 76 and 78 (Fig.13);
- forming a capacitor comprising a lower electrode 62, a capacitor dielectric 66 and an upper electrode 68 (Fig. 13);
- forming a conducting trench 64 to laterally extend the lower electrode 62 (Fig. 11), wherein the conducting trench 64 is electrically isolated from the upper electrode 68 and has a traverse dimension smaller than the traverse dimension of the capacitor (Fig.13); and
- forming two conducting pads 76 and 78 to contact with the upper electrode 68 and with the conducting trench 64, respectively (Fig.13), wherein the conducting trench 64 comprises the same conducting material as that of the lower electrode 62 (Fig.13).

With respect to claims 4, 5, 7, Brabazon et al also teach the steps of:

- forming the intertrack insulating layer 58 on the interlevel insulating layer 52 (Fig.10);
- etching a portion of the intertrack insulating layer 58 to form a cavity (Fig.10);
- forming a first conducting layer 62 to partially fill the cavity (Fig.11);
- forming the capacitor dielectric layer 66 on the first conducting layer 62 in the cavity (Fig.11);
- forming a second conducting layer 68 on the capacitor dielectric 66 to fill the cavity (Fig.12);

- forming an auxiliary trench 61 (Fig.10) and filling the auxiliary trench 61 with the first conducting layer 62 (Fig.11);
- chemical-mechanical polishing the first conducting layer 62, the capacitor dielectric 66 and the second conducting layer 68 to expose a top surface of the intertrack insulating layer 58 to form the capacitor 62/66/68 and the conducting trench 64 (Fig.12)

With respect to claims 12-18, Brabazon et al. also teach the claimed device having all the claimed limitations based on the method stated above, comprises : the metallization levels 10, 54, 56, 74, 76 and 78 are separated by interlevel insulating layers 52, 72; the intertrack insulating layer 72 separates the metallization 74, 76 and 78 at the same level; one capacitor comprises a lower electrode 62, a capacitor dielectric 66 and an upper electrode 68; the capacitor is located in at least part of the intertrack insulating layer 58 associated with the metallization level 76; the conducting trench 64 is electrically isolated from the upper electrode 68 and has a transverse dimension smaller than the transverse dimension of the capacitor; the interlevel insulating layer 72 covers the intertrack insulating layer 58; and two conducting pads 76 and 78 contact with the upper electrode 68 and with the conducting trench 64, respectively.

7. Claims 1-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Bernstein et al. (US 6,452,251).

With respect to claims 1, 2, 9, Bernstein et al identically teach the claimed method for fabricating an integrated circuit, the method comprising the steps of :

- forming a plurality of metallization levels, i.e. first metallization level 23, 25, second metallization level 41C/43B, 41/43C and third metallization level 75, 77 (Fig.1K)

wherein each of the metallization levels are separated by interlevel insulating layer 27, 29, 73 (Fig.1 K);

- forming the intertrack insulating layer 29, 73 to insulate each track of the same metallization level, i.e. forming the layer 29, 73 to insulate the metallization 41C/43B, 41/43C, 75 and 77 (Fig.1K);
- forming a capacitor comprising a lower electrode 41, a capacitor dielectric 49 and an upper electrode 51 (Fig. 1F);
- forming a conducting trench 41/43C to laterally extend the lower electrode 41 (Figs. 1F-1K), wherein the conducting trench 41/43C is electrically isolated from the upper electrode 51 due to the presence of an insulating layer 71 and has a traverse dimension smaller than the traverse dimension of the capacitor (Fig.1K); and
- forming two conducting pads 75 and 77 to contact with the upper electrode 51 and with the conducting trench 41/43C, respectively (Fig.1K), wherein the conducting trench 41/43C comprises the same conducting material as that of the lower electrode 41 (Fig.1K).

With respect claims 3, 6, 10, Bernstein et al. teach simultaneously forming the tracks of the metallization level 41/43B and the upper electrode 51 as shown in Fig. 1F.

With respect to claims 4, 5, 7, 11, Bernstein et al also teach the steps of:

- forming the intertrack insulating layer 29 on the interlevel insulating layer 27 (Fig.1B);
- etching a portion of the intertrack insulating layer 29 to form a cavity 35 (Fig.1B);
- forming a first conducting layer 41 to partially fill the cavity 35 (Fig.1C);

- forming the capacitor dielectric layer 49 on the first conducting layer 41 in the cavity 35 (Fig.1F);
- forming a second conducting layer 51 on the capacitor dielectric 49 (Fig.1F);
- forming an auxiliary trench 37 (Fig.1B) and filling the auxiliary trench 37 with the first conducting layer 41 (Fig.1D);
- forming a copper layer 53 on the upper electrode 51 and the conducting trench 41/43C (Fig.1F);
- chemical-mechanical polishing the copper layer 53 to expose a top surface of the layer 51 (Fig. 1G);
- etching a portion of the intertrack insulating layer 29 to form an auxiliary trench 39 (Fig.1B); and
- depositing the auxiliary trench 39 with a conducting layer 43B (Fig.1D).

With respect to claim 8, Bernstein et al. further teach that the width of the trench 37 (Fig.1B) is at least twice the thickness of the first conducting layer 41 (Fig.1D).

With respect to claims 12-18, Bernstein et al. also teach the claimed device having all the claimed limitations based on the method stated above, comprises : the metallization levels 23, 25, 41C/43B, 41/43C, 75, 77 are separated by interlevel insulating layers 27, 29, 73; the intertrack insulating layer 29, 73 separates the metallization 41C/43B, 41/43C, 75 and 77 at the same level; one capacitor comprises a lower electrode 41, a capacitor dielectric 49 and an upper electrode 51; the capacitor is located in at least part of the intertrack insulating layer 29 associated with the metallization level 75; the conducting trench 41/43C is electrically isolated from the upper electrode 51; the interlevel insulating layer 73 covers the intertrack insulating

layer 29; and two conducting pads 75 and 77 contact with the upper electrode 51 and with the conducting trench 41/43C, respectively.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 703-305-7341. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-0142 for regular communications and 703-305-0142 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Hsien Ming Lee
September 20, 2002

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800